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A 32x32 pixels vision sensor for Selective Change Driven readout strategy

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***Abstract*— The first VLSI vision circuit design following selective-change-driven (SCD) readout strategy is presented and simulated. Under this strategy, only pixels that exhibit large variations between the present and last transmitted illumination values are deemed to carry relevant information that is worth processing. Every pixel in a SCD VLSI implementation must be able to store and compare the present and the last transmitted illumination values. A subset of pixels exhibiting the largest variation between these two, should be read out in descending order of importance. This novel design accomplishes all these goals. Simulations on a 32x32 pixel matrix with sampling period of 500 μs and readout interval of 10 μs are presented. Average power consumption per pixel is in the order of 16 μW.**

I. Introduction

Frame-based imagers work under some very well known principles: the illumination level of the surrounding environment is sampled and transmitted at regular time intervals, even if no new information is produced. As such, a huge amount of redundant information is nevertheless processed and transmitted. Perfected over millions of years of evolution, biological vision systems work under a completely different basis. One of the key features of these systems, is that each sensor cell (pixel) reacts independently and asynchronously to illumination changes. Starting with Mahowalds's PhD work in 1992 [1], the last two decades have witnessed significant efforts towards overcoming the many limitations of frame-based vision sensors and algorithms - namely by incorporating biological neuromorphic principles into VLSI hardware design. Work like [1] and [2] pioneered in this field, together with, [3], [4] and [5] show successful implementations of neuromorphic vision systems. Results in this field clearly show that bandwidth and processing power needs are substantially reduced when neuromorphic principles are applied.

Within this framework, a new readout strategy is proposed in [6]. Such a selective change-driven (SCD) system is based on the idea that a pixel showing a large change in intensity is an indicator of fast movements and object edges around it. Usually, fast movements and edges (high spatial/temporal frequencies) are the most interesting parts of a scene. In the proposed strategy, successive snapshots of the environment are taken at a fast pace, but pixel readout is performed in an entirely different manner. Pixels are now transmitted out of the chip in descending order per their illumination level difference with respect to the last transmitted value. When a pixel's address and illumination information are transmitted, the illumination value is stored in a memory within the chip so the next forthcoming value can be compared against it. Pixel readout frequency can now be adapted to bandwidth availability. In the worst case scenario, one single pixel is transmitted, this being the one with the largest illumination change in the entire scene.

While the validity of SCD readout has been extensively discussed in [6], the benefits of its application to computer vision algorithms have been clearly demonstrated by MATLAB simulations in [7]. The purpose of this paper is to advance one step further by showing the first VLSI circuit design with SPECTRE simulations towards a silicon implementation.

In the transistor level implementation, the difference between the present and the previous illumination levels is physically represented as the output current of a wide-input-range operational transconductance amplifier (OTA) [8]. According to the SCD readout strategy, a subcircuit is needed to select the maximum amongst all these currents. Such a goal can be accomplished by a winner-takes-all (WTA) circuit [9] [10] [11] [12]. If we picture a WTA circuit as a black box, we'll see that a set of currents is taken as input, and a set of voltages is produced as output. Every output voltage is associated to a single input current. Ideally, the output voltage associated to the highest input current should be well differentiated from the rest. According to the current polarities in our light sensing circuit, the winning pixel should output a voltage close to 0V while the losers' output should be close to `Vdd`.

Given the always-limited discrimination ability of the WTA circuit, a large number of pixels increase the probability of having a certain number of cells competing with equal credentials. Therefore, multiple winners can be observed at the output nodes of the WTA amplifiers. To cope with this scenario, [13] proposes a digital logic based on the propagation of vertical and horizontal inhibition signals. Following a predefined path across the pixel matrix, inhibition signals are propagated so when the first winning output is found, the following outputs in the propagation path are forced to be close to `Vdd`. In favor of saving silicon area at the pixel level, only horizontal inhibition

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signals are used in this particular work; but the general idea of the inhibiting mechanism remains the same.

In Section II a description of the pixel circuit is introduced. Afterwards, Section III, shows the simulation of a 32x32 pixel matrix implementation in SPECTRE. Finally, we summarize our conclusions and depict a frame of reference for future work on the subject.

II. Pixel circuit

A. Light sensing and OTA subcircuits

As Fig. 1 shows, the light sensing subcircuit is based on a linear photocircuit [14]. The three main components of the photocircuit are the photodiode (whose very well known function is to transduct an incident light intensity into a photocurrent) and two capacitors: $C_{present}$ and $C_{previous}$. The function of $C_{present}$ is to store the present illumination value as a voltage once the parasitic capacitance of the photodiode is discharged by the photocurrent. $C_{previous}$ stores the pixel's last read out value. Signal `WTAfeedback` is fed back from the output of the digital logic of the WTA subcircuit; in this way, only the pixel showing the largest illumination variation is read out at `Vreadout` node, and the voltage at its $C_{previous}$ capacitor is updated. Transistor `MPROUT` and node `Vreadout` are common to the whole pixel matrix.

A wide-input-range OTA [8] is used to sense the voltage difference between $C_{present}$ and $C_{previous}$. OTA's output current can be positive or negative depending on wehther there has been an increase or decrease in the illumination level. According to the SCD strategy we are only interested in the absolute value of this variation, therefore this current has to be fully rectified [15]. Given this, the rectified output current of the OTA subcircuit for a particular pixel is a direct measure of the difference between the last sensed and the last read out illumination values.

B. WTA subcircuit

As explained previously, according to the SCD strategy the largest of the rectified currents should be selected. We accomplish this goal using a mixed analogue/digital WTA circuit implementation, depicted in Fig. 1.

All analogue WTA amplifiers are connected to the common node labelled `WTAcommon`, along with `Itail` current source. During normal operation, in case of a single winner cell, transistor `MP4` conveys the total `ITail` current while remaining in the saturation region. For the defeated cells, the current throughout the `MP4` transistor is negligible ($<<$ `ITail`) and transistor `MP1` is forced to work in the linear region with its `Vds` close to zero. As a result the `WTAout` node is close to `Vdd` in the loser cells and close to 0 V in the winning cells.

Transistors `MP1`, `MP2` and `MP3`, and current source `IPol`, form a gain-boosted regulated-cascode configuration whose only objective is to increase the resolution of the analogue WTA by increasing the impedance at `WTAout` node. An in-depth description of the analogue subcircuit is provided in [11].

The subcircuit labelled as `WTA digital logic`, generates a horizontal inhibition signal that follows the propagation path depicted in Fig. 2. Assuming that a logic "1" is a voltage close to `Vdd` and a logic "0" is close to 0 V, all `InhibitForward` signals in the path are sequentially asserted to "1" until the first winning cell is found. The first winning cell pulls `Verdict` signal to "0", and propagates an `InhibitForward` signal of "0". The logic gates that follow in the propagation path have inputs `InhibitPrevious`=0 and output `Verdict` set to "1". Only one single cell, the first winner found in the propagation path, has its `Verdict` signal in a low state.

Transistors `MPinv`, `MNinv` and `MNstarved` form a starved inverter that acts as a single bit analogue/digital interface presenting high impedance to the analogue output.

Care must be taken so the charge at $C_{previous}$ capacitor is updated for the winning pixel only. Transmission gates `TXG1` and `TXG2`, and inverters `INVA` and `INVB`, form a D latch whose objective is to feed a stable `WTAfeedback` signal into the photocircuit.

III. Simulations and results

A matrix of 32 x 32 pixels is simulated with the SPECTRE circuit simulator using models provided by austriamicrosystems 0.35 μm CMOS technology. The periods of `CKphd` and `CKwta` clock signals are set to 500 μs and 10 μs respectively. Fifty (50) pixels are read out per light sampling period, which, according to the SCD concept, are the most interesting ones. Two thousand (2000) light samples per second are taken. The average power consumption per pixel is in the order of 16 μW. `Vdd`=3.3 V.

In previous work with SPECTRE simulations [13] we show how the implemented WTA analogue/digital subcircuit efficiently handles a multiple winner situation by selecting a single winner with a resolution in the order of 10 nA. The results provided herein are focused on the manner in which winning pixels are read out and on how the voltage on there $C_{previous}$ capacitor is correctly updated.

The whole process is shown in Fig. 3 for pixel (29,22). This pixel was chosen for no special reason other than for being one of the multiple winners at some point in the simulation. If rows and columns are numbered in the range $0 \ldots 31$, and the inhibiting propagation path is the one depicted in Fig. 2, then cell (29,22) inhibits cell (29,21), and cell (29,23) inhibits cell (29,22). This last pixel has its $\texttt{WTAout}_{(29,22)}$ signal at a low state, which means that it belongs to the multiple winners' subset. When the simulation reaches 1.01 ms, signal $\texttt{InhibitPrevious}_{(29,22)} = \texttt{InhibitForward}_{(29,23)}$ is pulled high. Since $\texttt{WTAout}_{(29,22)}$ is in a low state, $\texttt{Verdict}_{(29,22)}$ falls to low leaving pixel (29,22) as the only winner in the matrix. In the next pulse of `CKwta`, at 1,02 ms, $\texttt{WTAfeedback}_{(29,22)}$ is pulled low. Voltage at $C_{present(29,22)}$ is copied to $C_{previous(29,22)}$ and voltage at `Vreadout` is transmitted out of the chip. Differential voltage at $OTA_{(29,22)}$'s subcircuit input, now registering 0 V, produce a negligible $\texttt{Irect}_{(29,22)}$ output current.

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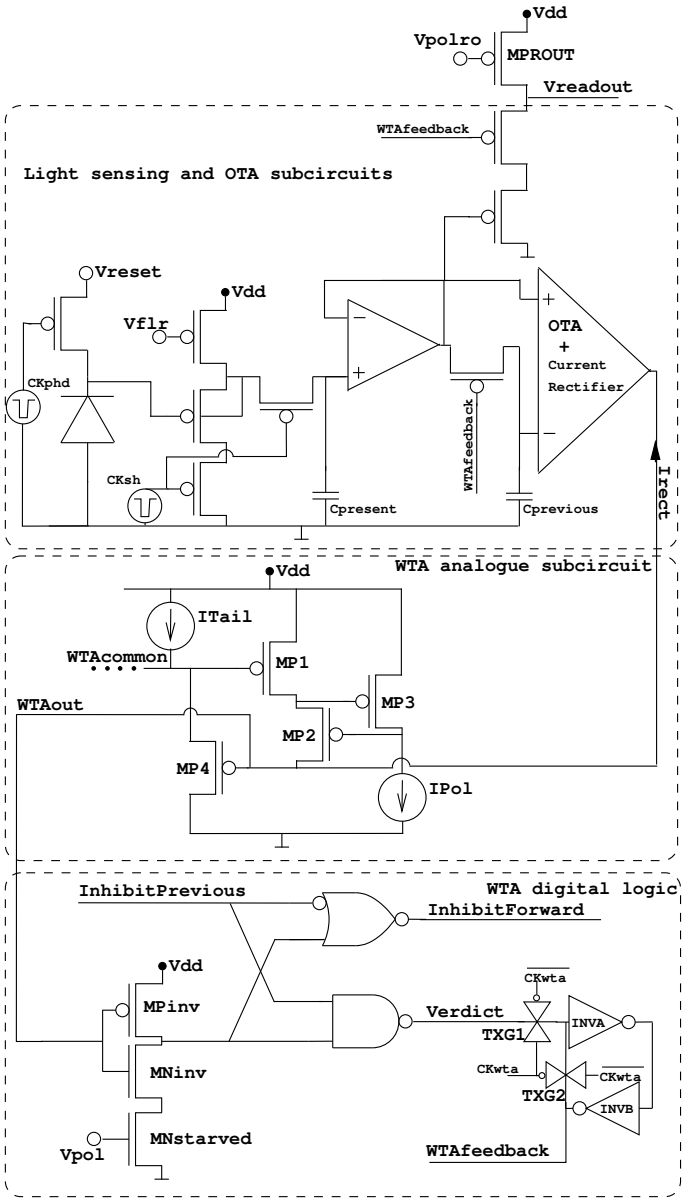

Fig. 1. Schematic of the pixel circuit.

The updated cell now loses the contest at WTA subcircuit and $\texttt{InhibitForward}_{(29,22)}$ is pulled high permiting cell (29,21), the next multiple winner in the inhibiting path, to become a single winner in the matrix.

IV. Conclusion

We have described a novel circuit for vision VLSI chips, this being the first VLSI design that follows the basis of SCD strategy. Pixels that exhibit large variations between the present illumination value and the last transmitted one are the only ones considered relevant and are therefore read out in descending order of importance. Since focus is being put on those pixels that show relevant (new) information, the circuit can be considered as following the principles of neuromorphic vision system designs.

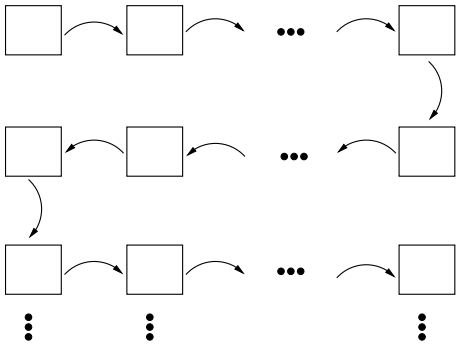

Fig. 2. Propagation path for inhibition signals.

The light sampling interval is 500 μs. Simulations show how, every 10 μs, the circuit pinpoints the pixel with the largest change in illumination amongst the entire pixel matrix. Hence, only the most relevant information is selected and then transmitted out of the chip for processing purposes. As a result, an equivalent velocity of 2000 frames per second is achieved, facilitating the processing of high-speed movements without the need of large bandwith or high computing power.

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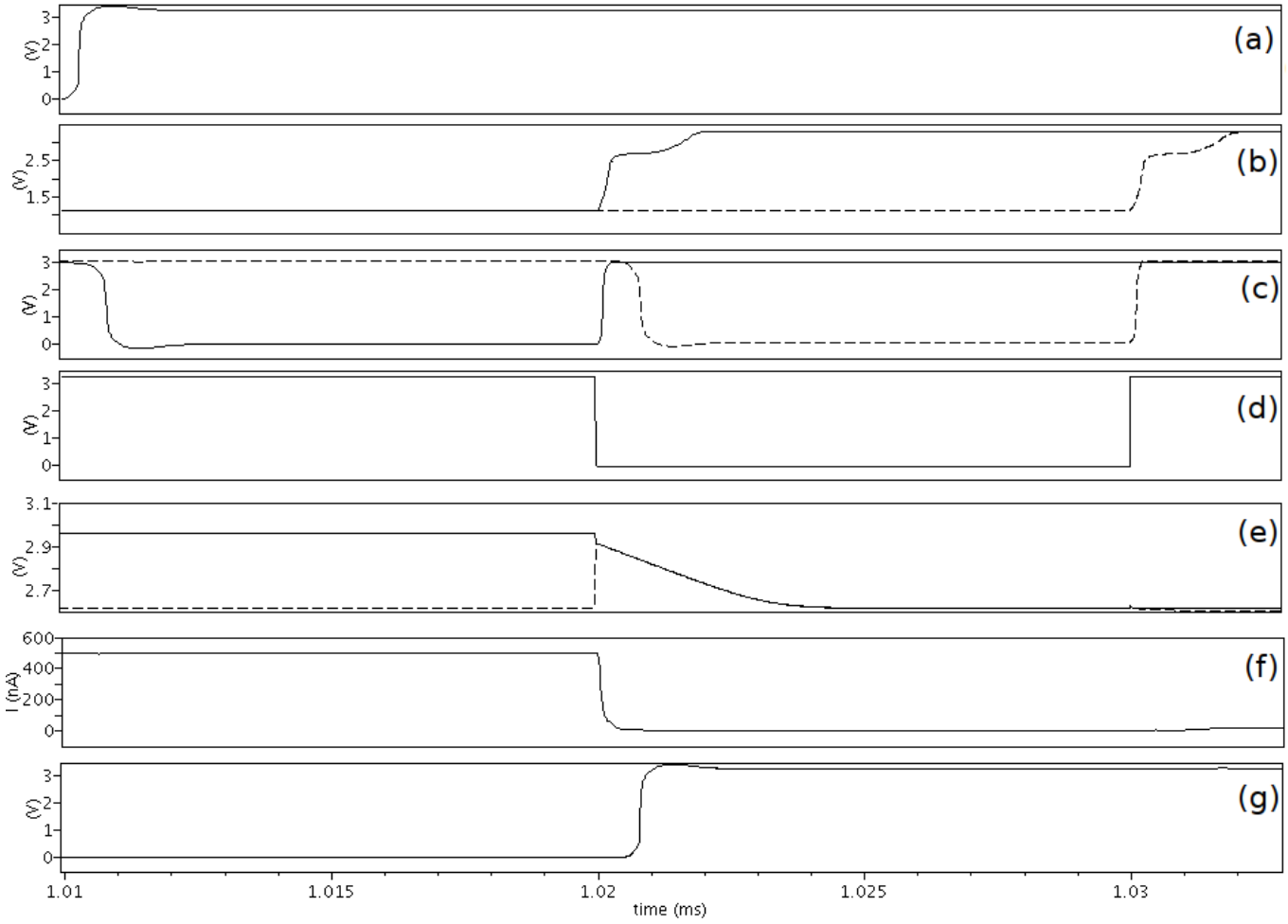

Fig. 3. (a)$\texttt{InhibitForward}_{(29,23)} = \texttt{InhibitPrevious}_{(29,22)}$, (b) $\texttt{WTAout}_{(29,22)}$ (solid) and $\texttt{WTAout}_{(29,21)}$ (dashed), (c) $\texttt{Verdict}_{(29,22)}$ (solid) and $\texttt{Verdict}_{(29,21)}$ (dashed), (d) $\texttt{WTAfeedback}_{(29,22)}$, (e) voltage at $C_{previous(29,22)}$ (solid) and $C_{present(29,22)}$ (dashed), (f) $\texttt{Irect}_{(29,22)}$, and (g) $\texttt{InhibitForward}_{(29,22)}$.